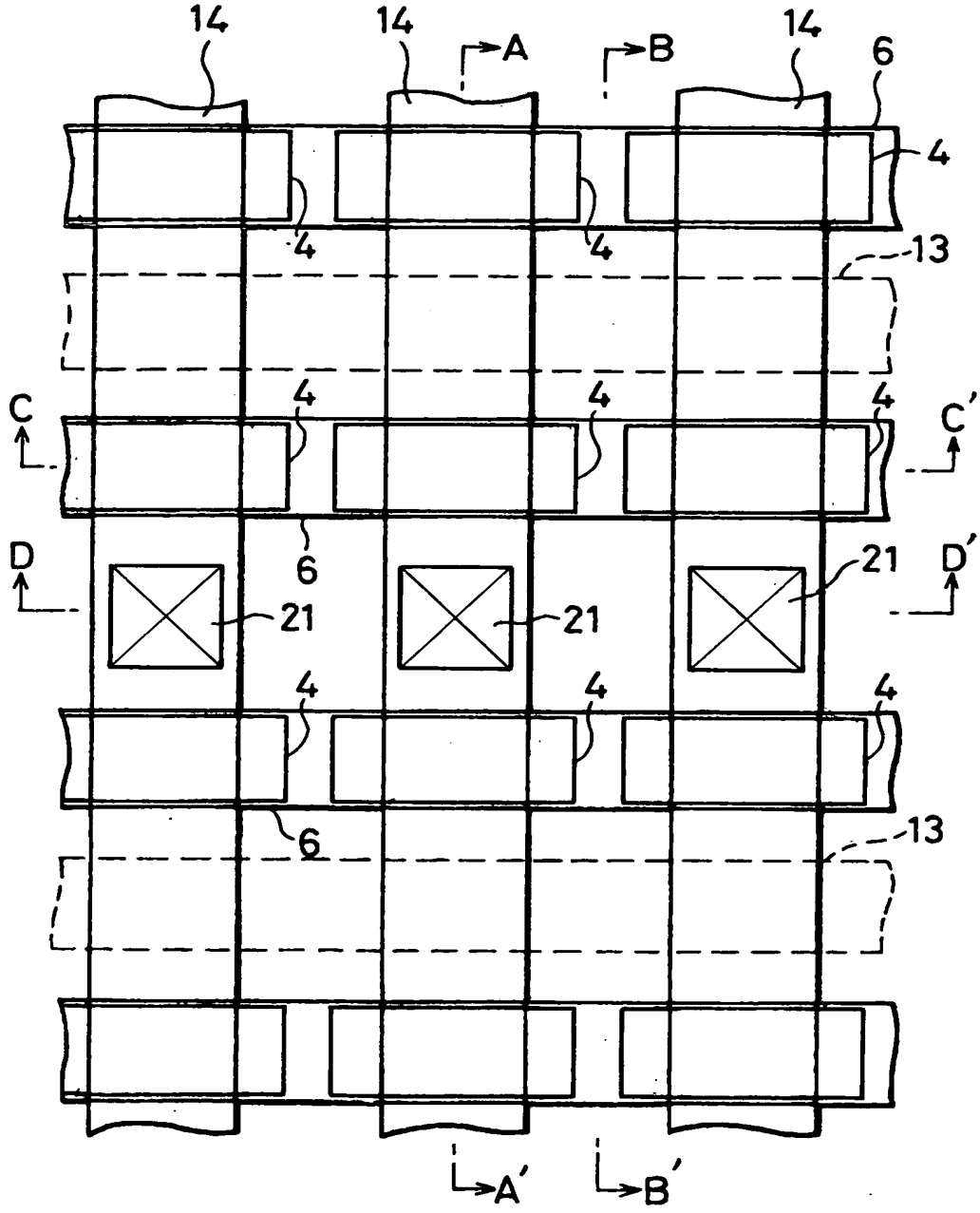


FIG. 1

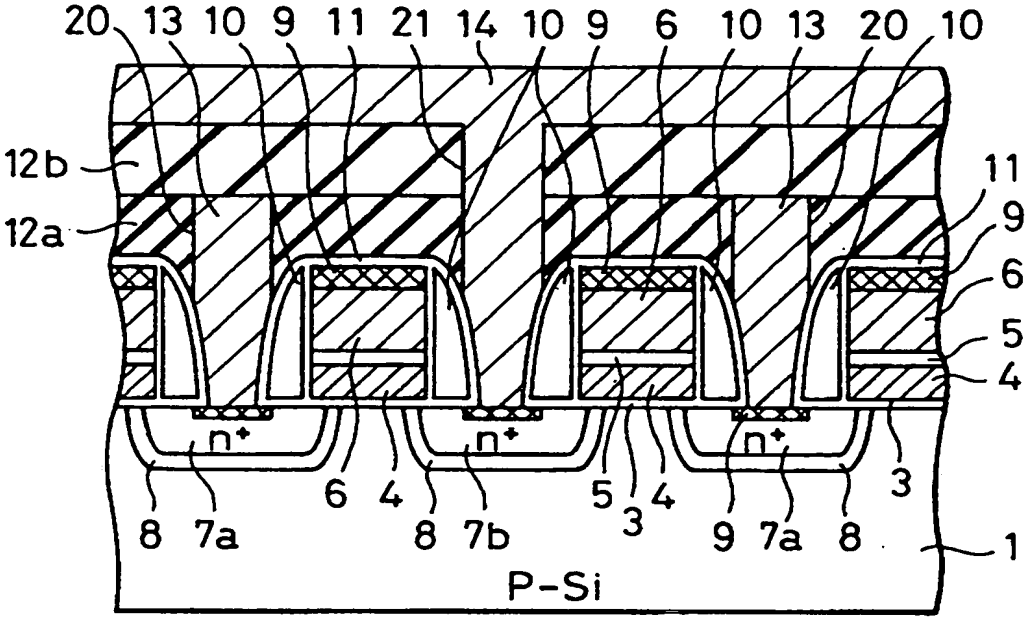

20
13
10
9
11
21
14
10
9
6
10
13
20
10
12b
12a
11
9
6
5
4
n+
n+
n+
8
7a
6
4
8
7b
5
3
4
9
7a
8
3
1
P-Si

FIG. 2 (a)

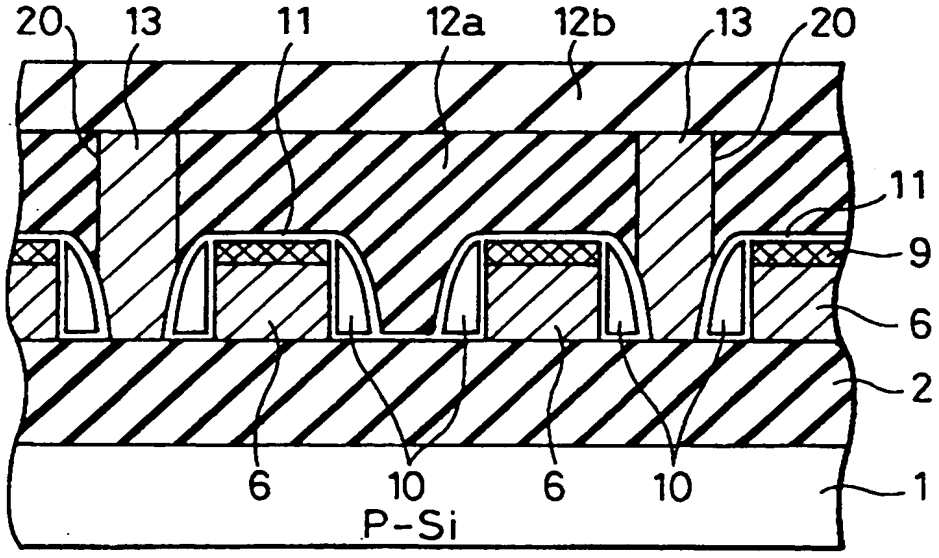

20
13
11
12a
12b
13
20
11
9
6
2
6
10
6
10
1
P-Si

FIG. 2 (b)

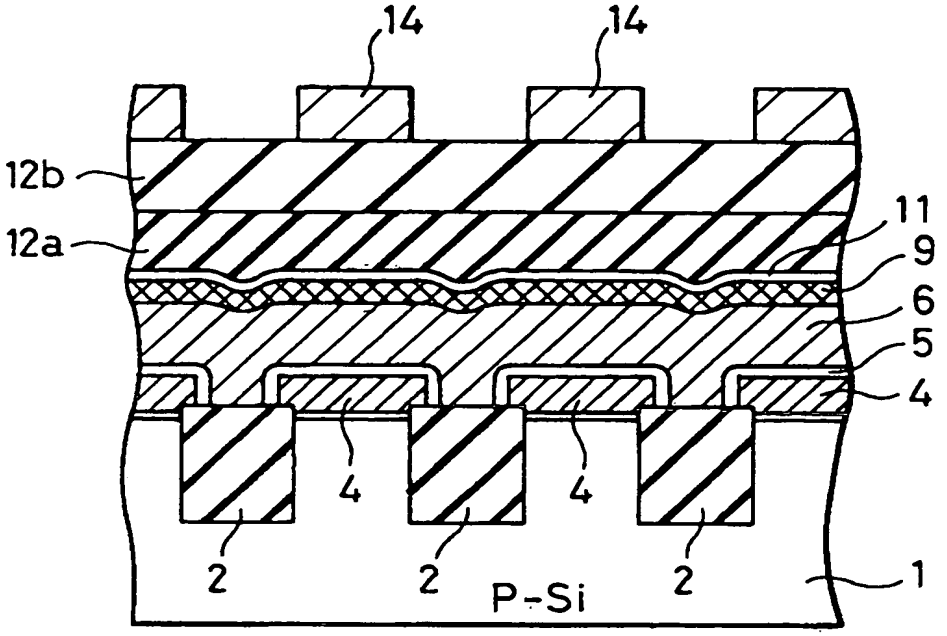

14
14
12b
12a
11
9
6
5
4
4
4
2
2
2
P-Si
1

FIG. 3 (a)

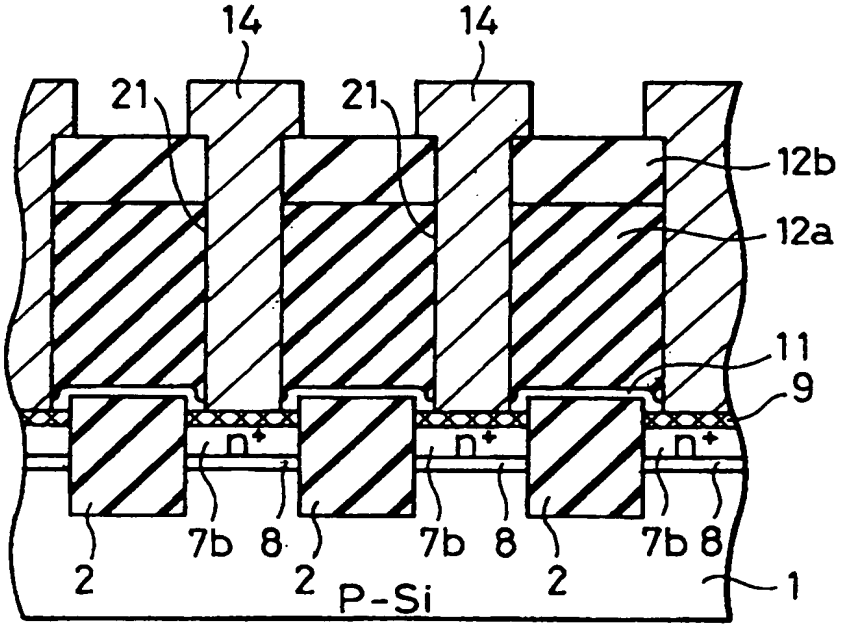

14
14
21
21
12b
12a
11
9
n+
n+
n+
7b
8
7b
8
7b
8
2
2
2
P-Si
1

FIG. 3 (b)

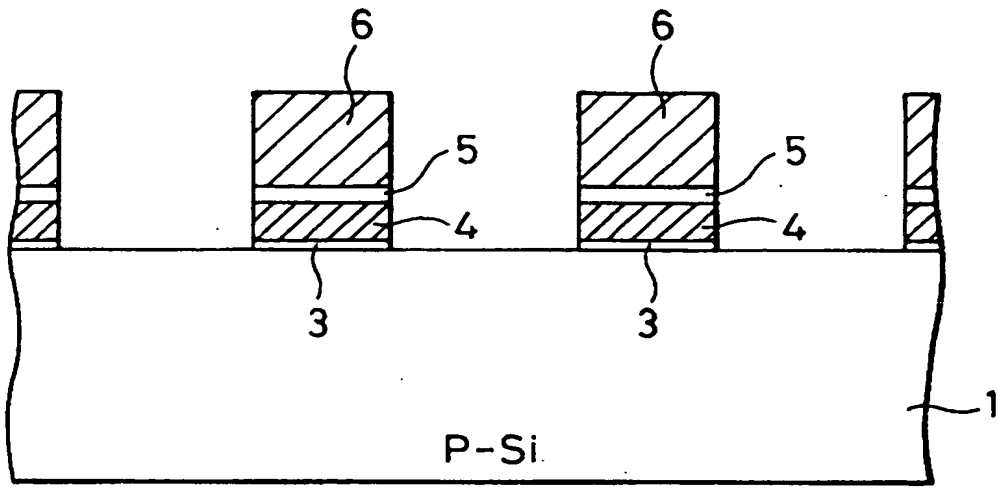


FIG. 4 (a)

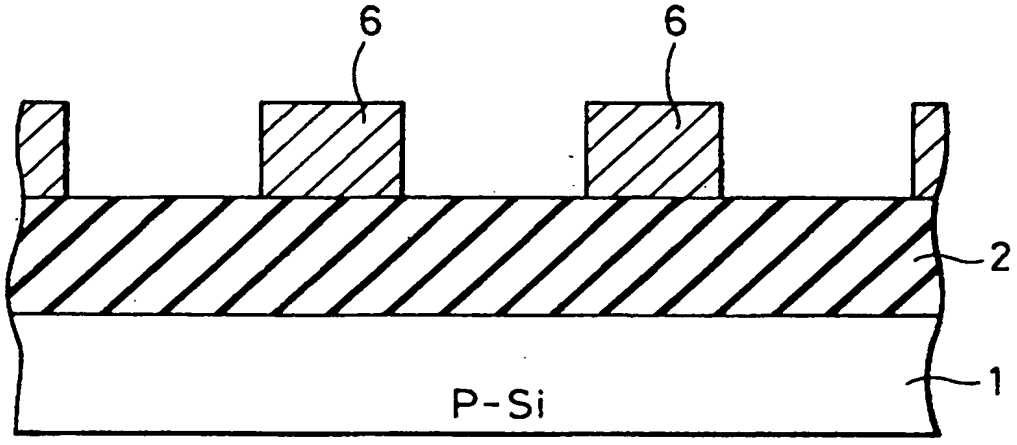


FIG. 4 (b)

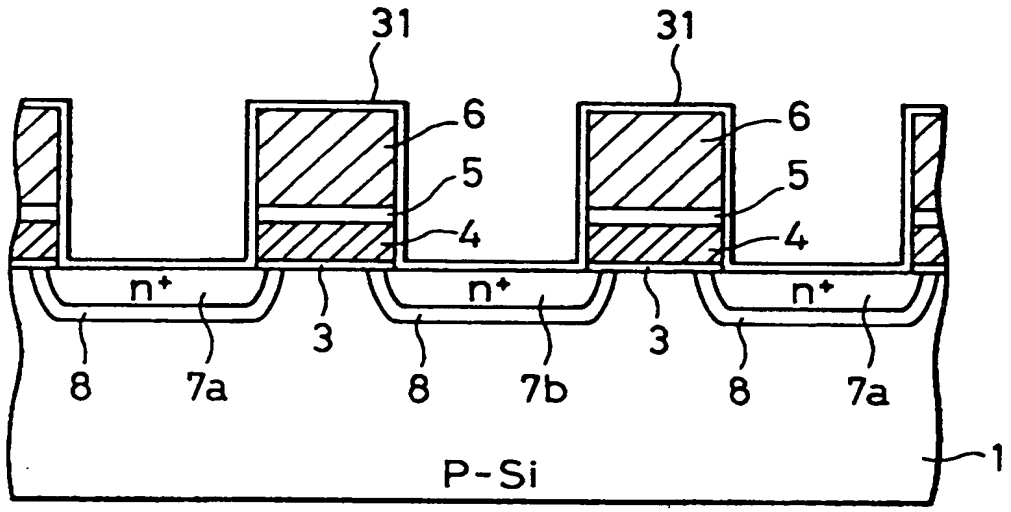


FIG. 5 (a)

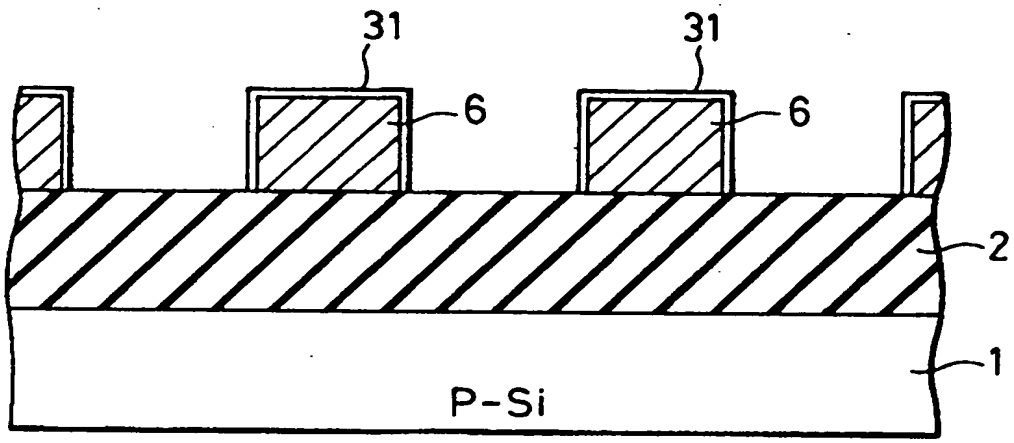


FIG. 5 (b)

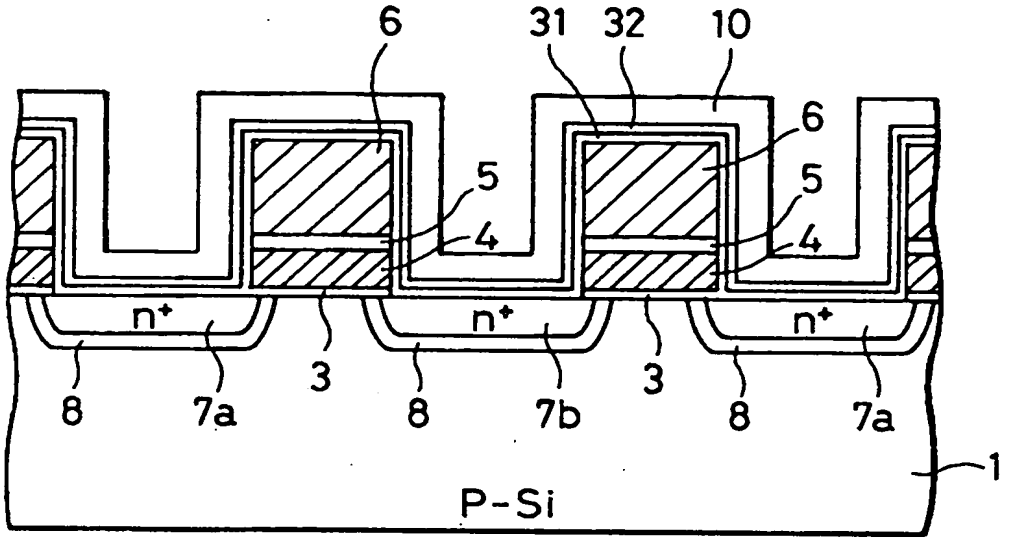


FIG. 6 (a)

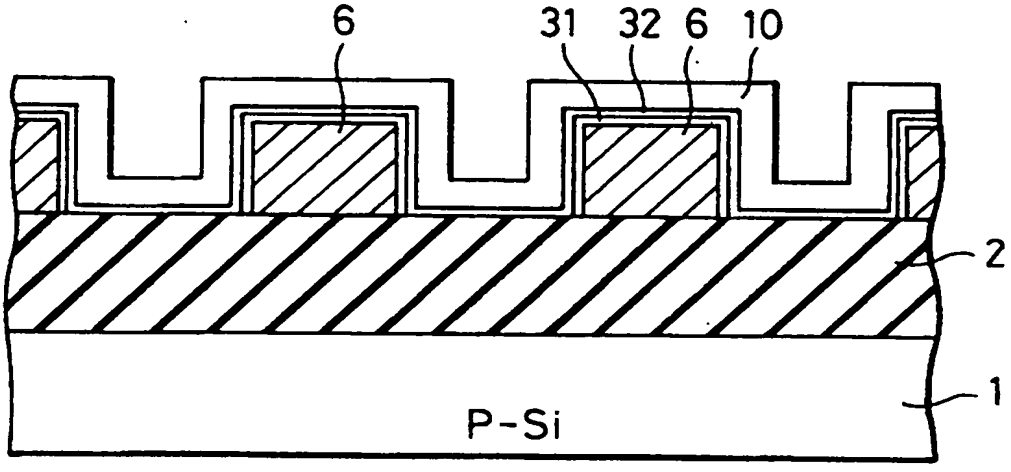


FIG. 6 (b)

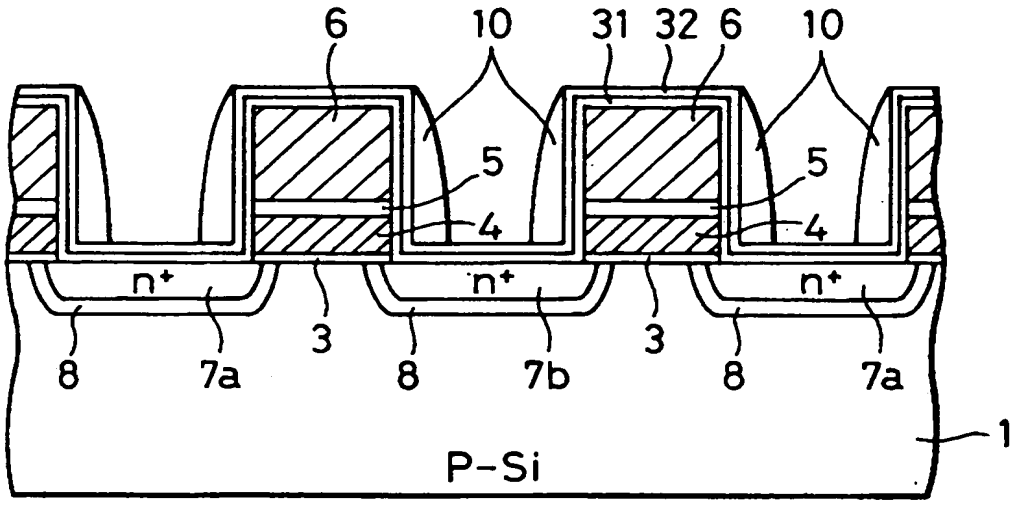


FIG. 7 (a)

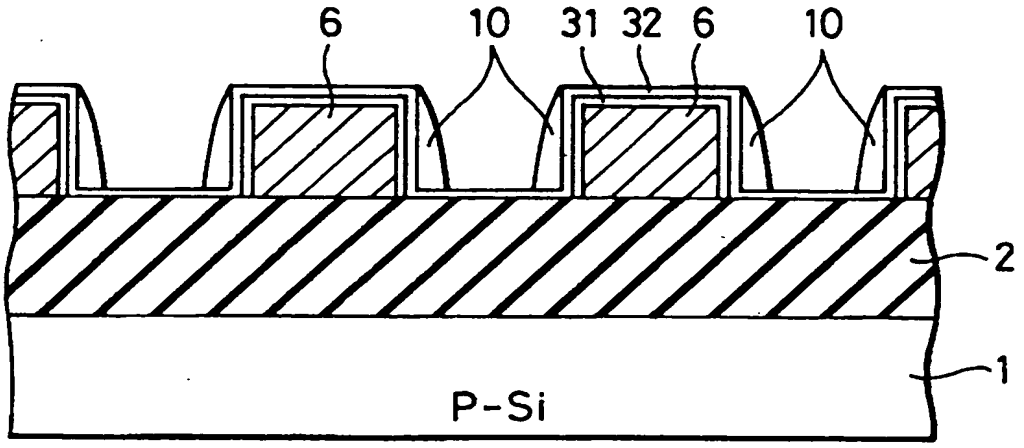


FIG. 7 (b)

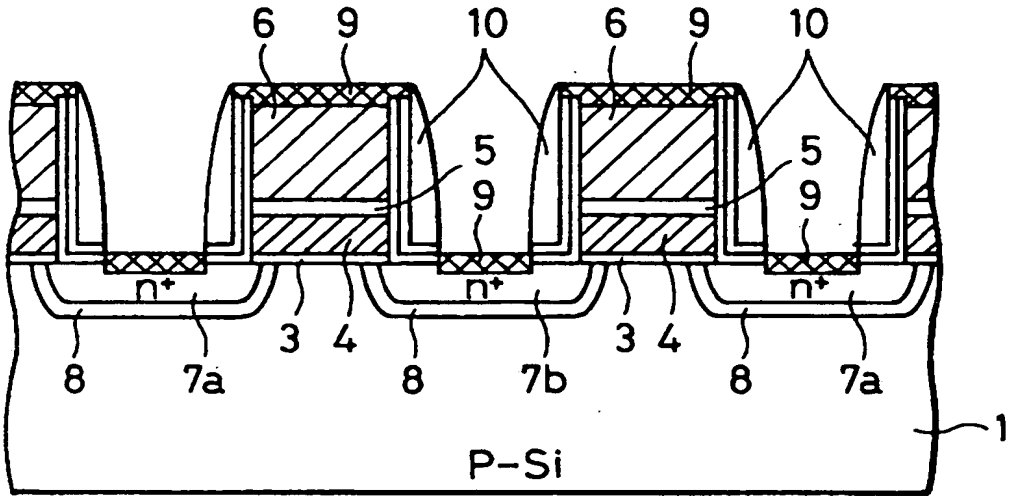


FIG. 8 (a)

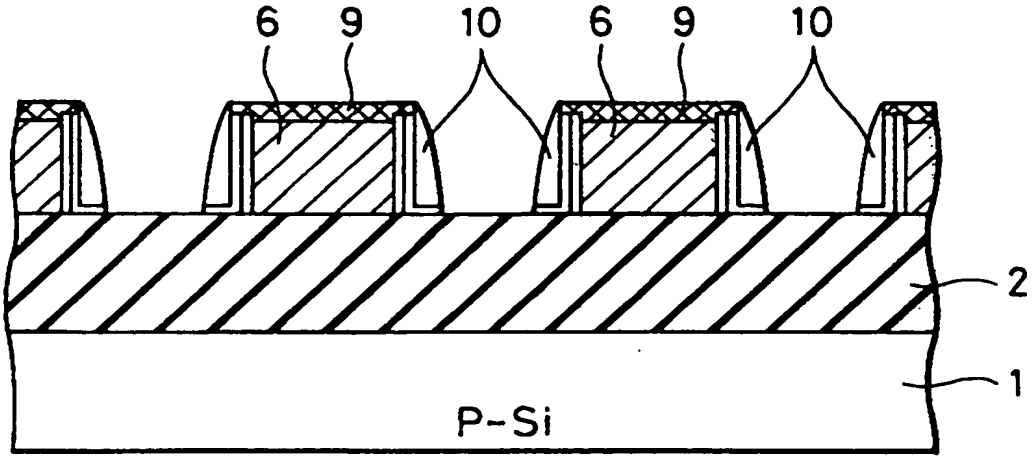


FIG. 8 (b)

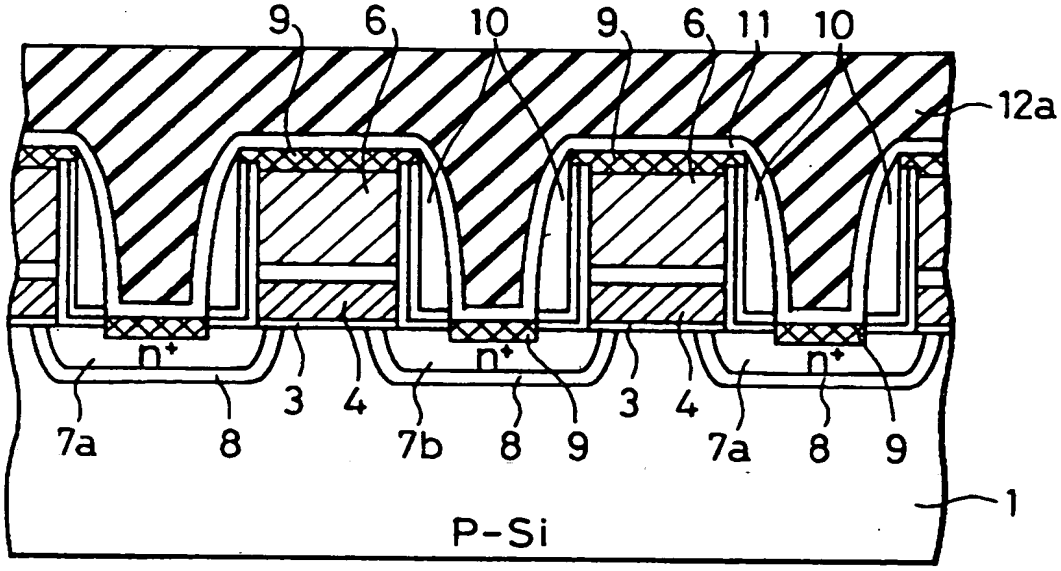

9
6
10
9
6
11
10
12a
n+
n+
n+
3
4
3
4
7a
8
7b
8
9
7a
8
9
1
P-Si

FIG. 9 (a)

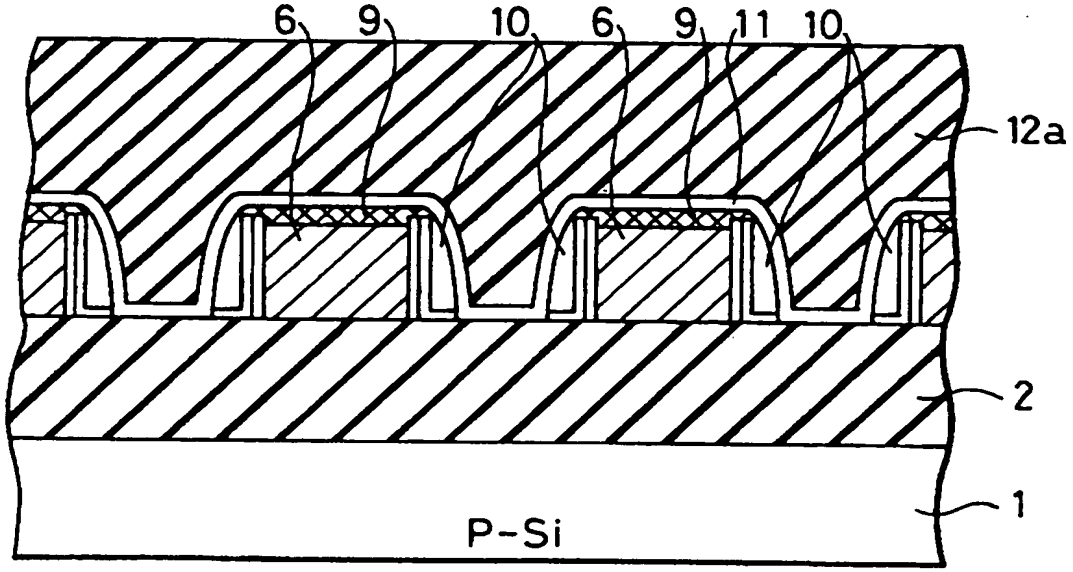

6
9
10
6
9
11
10
12a
2
1
P-Si

FIG. 9 (b)

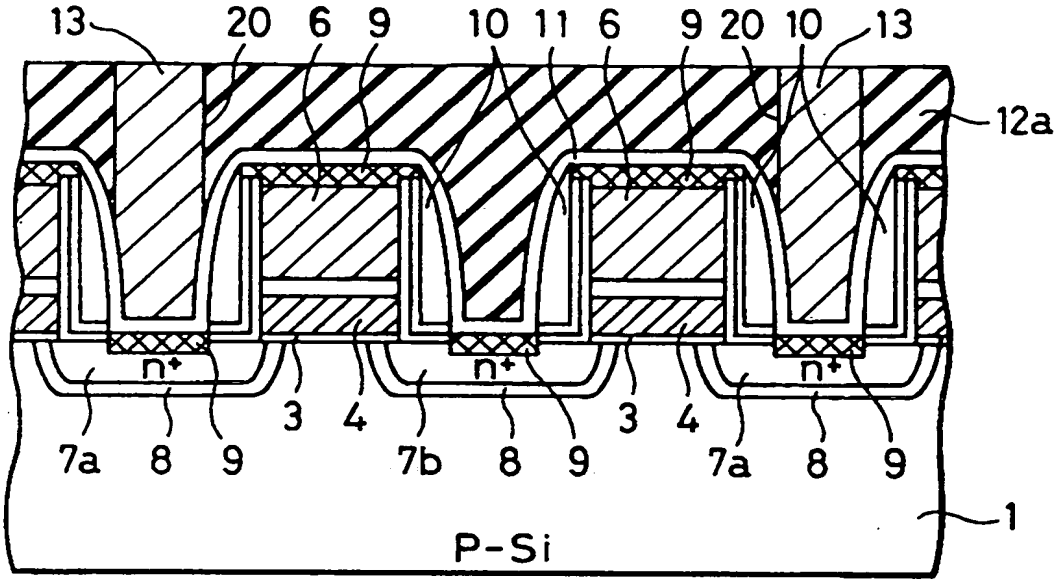


FIG. 10 (a)

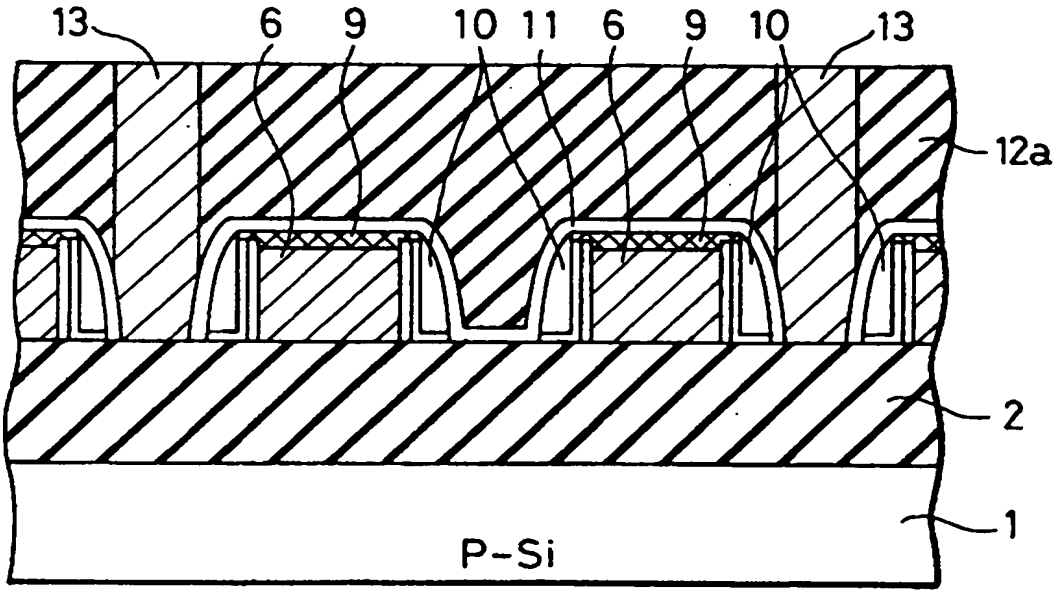


FIG. 10 (b)

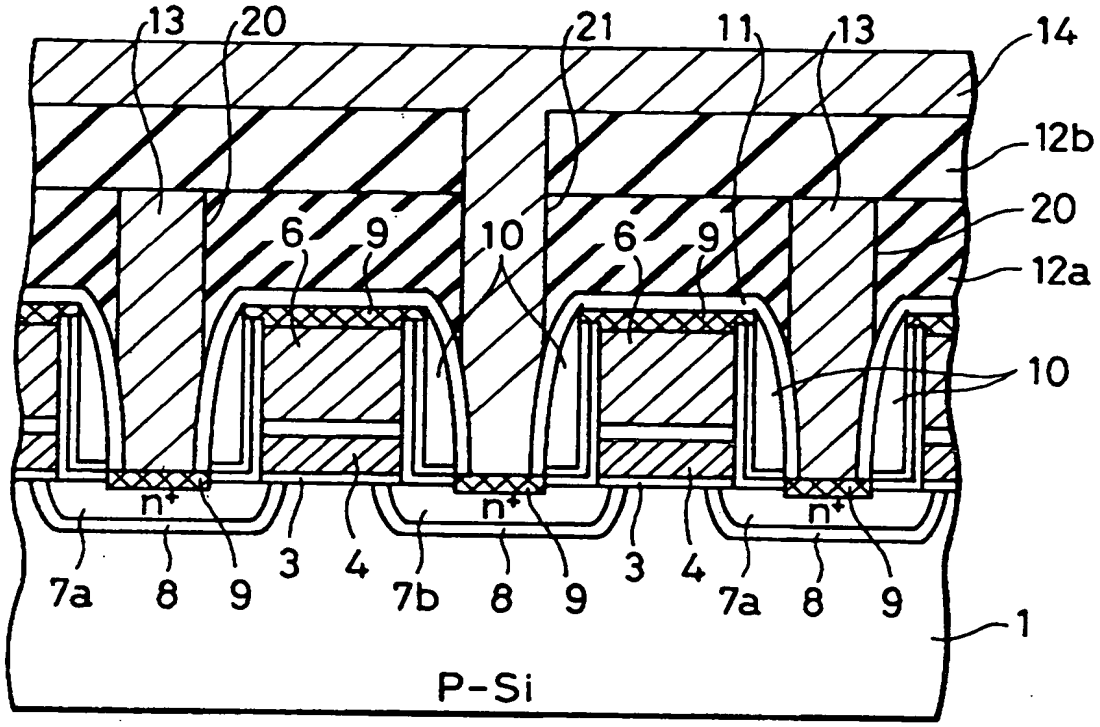


FIG. 11 (a)

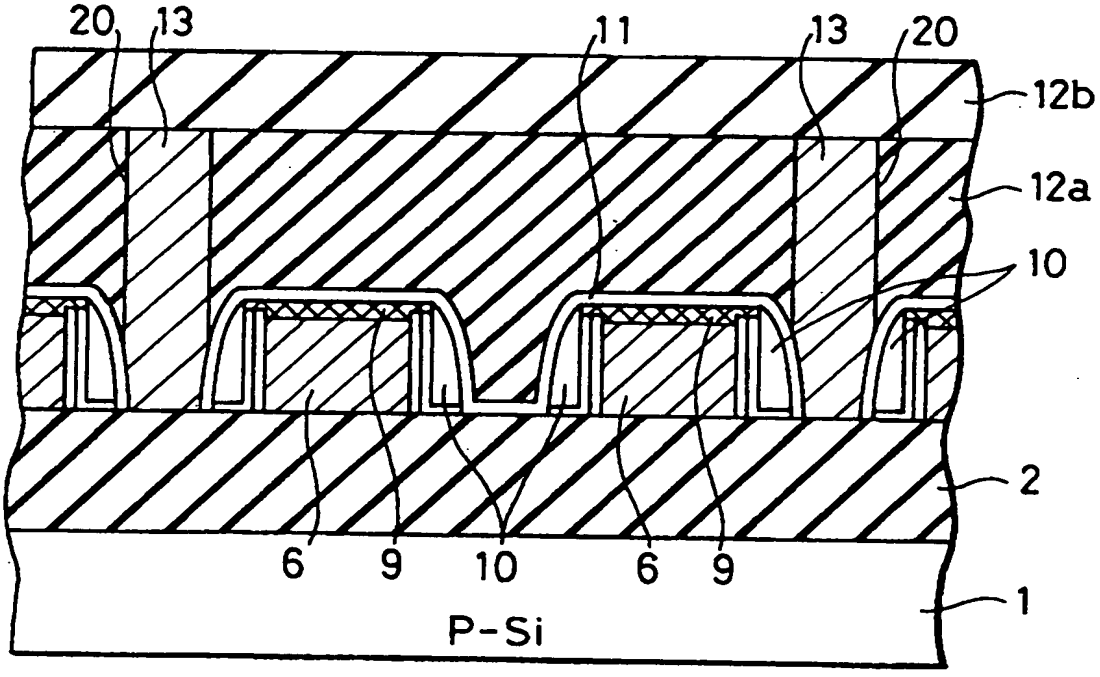


FIG. 11 (b)

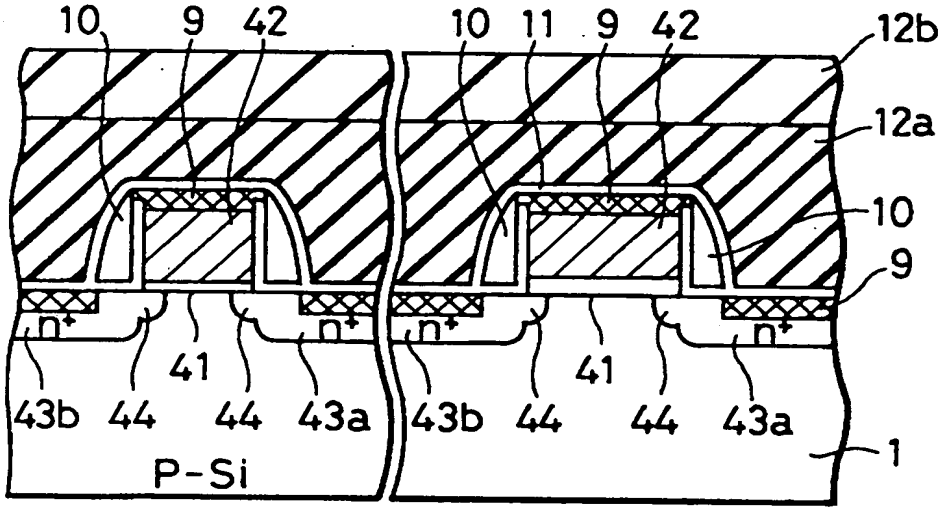

10
9
42
10
11
9
42
12b
12a
10
9
n+
n+
n+
n+
41
41
43b
44
44
43a
43b
44
44
43a
P-Si
1
[LOW-VOLTAGE MOS]
[HIGH-VOLTAGE MOS]

FIG. 12

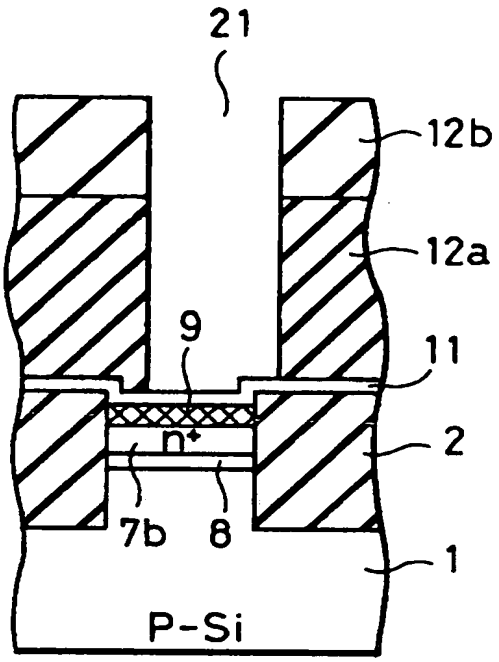


FIG. 13

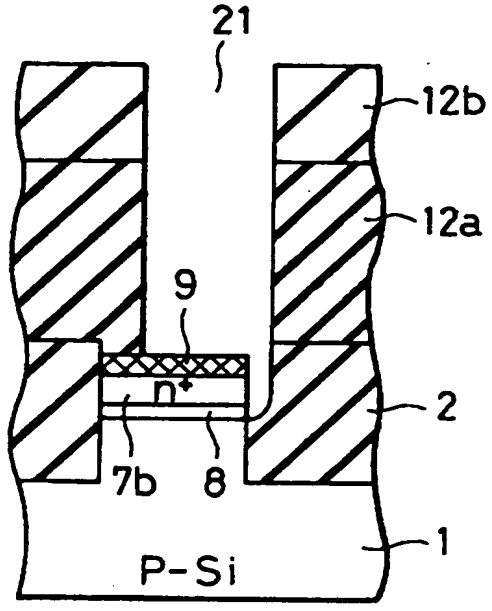
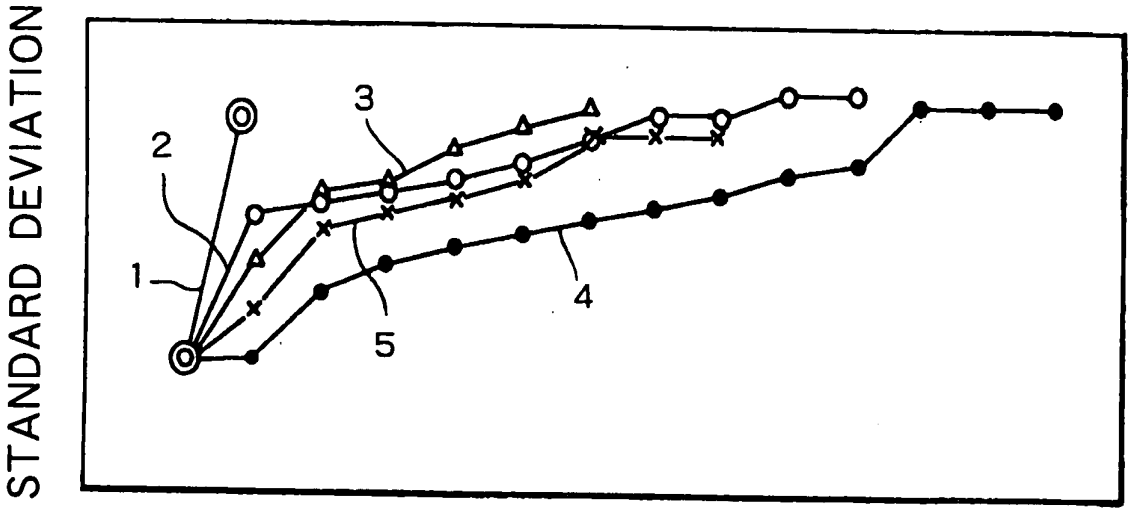


FIG. 14



1 : INITIAL VALUE
2 : COMPARATIVE EXAMPLE 1
3 : COMPARATIVE EXAMPLE 2
4 : COMPARATIVE EXAMPLE 3
5 : EMBODIMENT OF THE PRESENT INVENTION

o—o SIDE WALL SiO_2
Δ—Δ SIDE WALL SiN
●—● SIDE WALL SiO_2+P.SiN
×—× SIDE WALL SiN +P.SiN

FIG. 15